R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

IN THE DRAWINGS

The objection to the drawings is traversed. FIG. 2 illustrates an example of a functional portion with the FPGA core 116 and a logic portion with the combinational logic 130. Therefore, the objection to the drawings should be withdrawn.

CLAIM OBJECTIONS

The objection to claims 1, 10 and 21 under 35 U.S.C. §112 has been obviated by appropriate amendment and should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of (i) claims 1-27 under 35 U.S.C. §102(e) as being anticipated by Killian '683, (ii) claims 1-3 and 26 under 35 U.S.C. §102(b) as being anticipated by Amini '373, (iii) claims 1-3, and 26-27 under 35 U.S.C. §102(b) as being anticipated by Dapp '152 and (iv) claims 1-3 and 26-27 under 35 U.S.C. §102(e) as being anticipated by Winegarden '009 has been obviated by appropriate amendment and should be withdrawn.

Claim 1 of the present invention provides a system for designing an integrated circuit (IC). The system generally

comprises a functional portion, a logic portion, a debugging/fix circuit and a diagnostic architecture. The logic portion generally includes one or more interfaces. The programmable portion may be configured to detect, correct and/or diagnose errors in the logic portion through the one or more interfaces. The debugging/bug fix circuit may be configured to detect errors in the logic portion. The diagnostic architecture may use the FPGA core in a system on a chip design.

The references do not disclose or suggest each and every element of the presently claimed invention. In particular, none of the references appear to disclose or suggest a diagnostic architecture, as presently claimed. As such, claim 1 of the present invention is fully patentable over the cited references and the rejection should be withdrawn.

Claim 26 of the present invention provides a method for diagnostics comprising the steps of (A) interfacing a chip with an FPGA core, (B) presenting one or more internal signals of the chip, (C) verifying or fixing bugs in the chip with the one or more internal signals and (D) programming the FPGA core to dump data from a host register every N clock cycles. The references are silent regarding at least the step of processing the FPGA core to dump data from a host register every N clock cycles. As such, claim 26 is fully patentable over the cited references and the rejection should be withdrawn.

Claims 2-24 and 26 depend, directly or indirectly from the independent claims, which are now believed to be allowable. Newly presented claims 28-33 are believed to be independently patentable over the cited references.

As such, the presently claimed invention is fully patentable over the cited references and the rejection should be withdrawn.

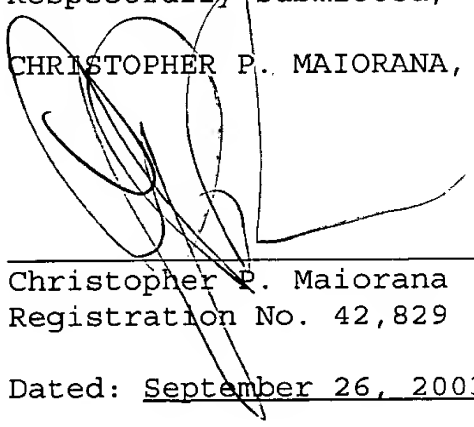
Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative at 586-498-0670 should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge Deposit Account No. 12-2252.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.



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